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Windowless CdSe/CdTe Solar Cells with Differentiated Back Contacts: *J*–*V*, EQE, and Photocurrent Mapping

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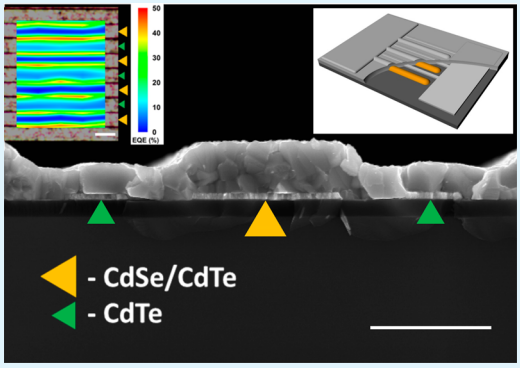
ABSTRACT: This study presents windowless CdSe/CdTe thin film photovoltaic devices with in-plane patterning at a submicrometer length scale. The photovoltaic cells are fabricated upon two interdigitated comb electrodes prepatterned at micrometer length scale on an insulating substrate. CdSe is electrodeposited on one electrode, and CdTe is deposited by pulsed laser deposition over the entire surface of the resulting structure. Previous studies of symmetric devices are extended in this study. Specifically, device performance is explored with asymmetric devices having fixed CdTe contact width and a range of CdSe contact widths, and the devices are fabricated with improved dimensional tolerance. Scanning photocurrent microscopy (also known as laser beam induced current mapping) is used to examine local current collection efficiency, providing information on the spatial variation of performance that complements current–voltage and external quantum efficiency measurements of overall device performance. Modeling of carrier transport and recombination indicates consistency of experimental results for local and blanket illumination. Performance under simulated air mass 1.5 illumination exceeds 5% for all dimensions examined, and the best-performing device achieved 5.9% efficiency.



KEYWORDS: *back contact, CdSe, CdTe, photovoltaic, 3D solar cells, LBIC*

INTRODUCTION

This work examines thin film CdTe photovoltaic cells with a back contact geometry in which the positive and negative electrodes form an interdigitated comb structure on the rear of the device. Back contact geometry devices of crystalline Si have a long history in the literature.[1−3] Back contact thin film devices have been fabricated more recently.[4−8] The thin film devices require finer pitch electrodes due to shorter carrier recombination lengths. However, the back contact geometry removes the need for a transparent conducting oxide layer and bandgap restrictions imposed on the (*n*-type) junction layer for optical transparency.

Devices based on the CdTe/CdSe system are examined; previous studies have examined back contact devices based on this system[7,8] as well as the traditional CdTe/CdS system.[4] The fabrication process utilized herein, which involves a single patterning procedure to place both electrodes, has been detailed in earlier studies. Device level characterization includes current density–voltage (*J*–*V*) response under simulated air mass 1.5 (AM1.5) illumination as well as external quantum efficiency (EQE) using a spectrally filtered light source.

Spatial variation of conversion efficiency within the solar cells is assessed using scanning photocurrent microscopy, in this case, laser beam induced current mapping (LBIC), in which a focused optical beam is rastered across the device surface while device response is monitored. LBIC, while it has a lower resolution than electron beam induced current mapping techniques, is analogous to photovoltaic operating conditions in which equal numbers of minority and majority carriers are generated.[9,10] The technique has been used to study the impact of a variety of factors on device performance.[11] Among others, it has been used to characterize the photovoltaic performance of thin film and nanowire based devices,[12,13] as well as CdSe/CdTe back contact thin film devices[8] of the type studied here. The localized measurements are relevant to efforts aimed at

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improved device efficiency or utilization of more abundant, but typically lower quality, materials through light management strategies and advanced architectures. Such structures include plasmonic, quantum dot, and nanowire based devices,[13−17] as well as nonplanar contact and heterojunction structures.[18] While promising in theory, achieving even the efficiency of planar devices has proven to be challenging as is detailed in a comprehensive review of the use of elongated nanostructures.[19] Improved understanding of electron−hole pair generation and charge carrier transport in three-dimensional absorber materials using measurements such as those presented here will be required to obtain higher performance.

Because LBIC previously indicated higher performance over and around the CdSe contact lines of back contact CdSe/CdTe devices,[8] the width of these contacts (W_{CdSe}) is systematically varied in this study; the width of the CdTe contacts is held constant. Contact lines to both semiconductors were equally wide in previous studies of both CdS/CdTe and CdSe/CdTe back contact devices. Modeling of light absorption and associated carrier transport and recombination under both global and local illumination is used to understand the experimental results.

EXPERIMENTAL SECTION

Device Fabrication. The procedure for device fabrication is similar to that used to fabricate previous CdSe/CdTe back contact devices.[8] To summarize, the two interdigitated comb electrodes for each device were simultaneously patterned on an oxidized silicon wafer substrate. The asymmetric devices were patterned using a stepper system with 5:1 reduction from the mask; symmetric CdSe/CdTe back contact devices in previous studies were lithographically patterned using a contact mask. The specified ±0.25 μm dimensional tolerance of the masks, which transfers directly to the symmetric devices patterned with contact lithography, is reduced to 0.05 μm for the asymmetric devices produced using the stepper. Iridium was used for the electrodes as with the earlier devices. While the large work-function (approximately 5.5 eV[20]) should be reasonably well suited for the CdTe contact, a Schottky junction at the *n*-CdSe/Ir interface is likely detrimental to device performance. For the devices examined here, the distance between the midlines of adjacent contact wires on the two electrodes (i.e., electrode "pitch") is from 2 to 3 μm: W_{CdSe} is in the range of 1−3 μm, while the CdTe contact wires and the gap between adjacent CdSe and CdTe contact wires is 1 μm wide in all cases. The Ir contact wires are approximately 80 nm thick for all the asymmetric devices (W_{CdSe} > 1 μm) with contacts ranging from 50 to 80 nm for the symmetric devices (W_{CdSe} = 1 μm). The CdSe was electrodeposited on the desired electrode using an underpotential codeposition process[21,22] detailed previously for CdS,[4] CdSe,[7,8] and CdTe[4] for earlier back contact devices. Unlike in previous studies, the devices were rotated at 30 rpm in an attempt to improve the uniformity of the CdSe deposit thickness across the device. The CdSe thickness is between 0.3 and 0.5 μm thick, for which values shunting by pinhole formation through the CdSe layer during annealing is generally not a problem. Following electrodeposition of the CdSe the devices were rinsed, dried, and then annealed in a tube furnace at 500 °C for 10 min under a N_2 atmosphere. CdTe between 0.4 and 0.6 μm thick was subsequently deposited over the entire device by pulsed laser deposition for the asymmetric dies. Symmetric dies (W_{CdSe} = 1 μm) such as those previously studied[8] were fabricated with CdTe thickness between 0.7 and 1.1 μm thick using the same process described in the earlier study. After CdTe deposition, all devices were coated with $CdCl_2$ and annealed at 400 °C for 10 min in a nitrogen plus oxygen environment. Final processing involved immersion in 40% by mass (aq) ammonium sulfide at room temperature, rinsing in distilled water, and drying. Device performance was assessed after 30, 45, and 60 s of cumulative immersion.

Because fabrication of these dual back contacted devices starts with the positive and negative electrodes and finishes with the absorber, the finished devices have a fully exposed absorber surface. Figure 1 shows a schematic of the device geometry with scanning electron micrographs of a CdSe/CdTe device cross-sectioned after processing. The devices have an active area of 0.16 cm^2.

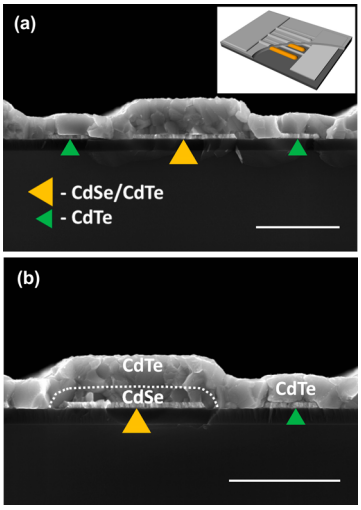

Figure 1. (a) Cross section SEM image of a CdSe/CdTe device with 2.5 μm wide CdSe contact and 1 μm wide CdTe contact, as well as gaps between contacts. The Ir contacts are approximately 80 nm tall. The device exhibits periodicity at twice the electrode pitch because of the CdSe deposit on every other wire. Arrows mark the locations of the wire contacts, and the scale bar is 2 μm. (Inset) Schematic of the device. The overlying CdTe is removed from a portion to show the CdSe on one electrode and the wires of the other electrode with the contact pad connecting them. (b) Higher magnification SEM image of the same device. The approximate CdTe/CdSe interface is indicated.

Characterization Methods. The microstructure and composition of the materials in the devices were examined using a scanning electron microscope (SEM). Planview images were taken without additional preparation. Cross sections were imaged from freshly cleaved samples.

Devices were characterized by standard *J*−*V* response under AM1.5 illumination as well as EQE measurements using a spectrally filtered light source. The illumination intensities in both cases were calibrated using a NIST-calibrated silicon photodiode. The current density (*J*) was obtained from the measured current using the 0.16 cm^2 active area of the devices. Uncertainty of the measurements is dominated by calibration of the light source and subsequent placement of devices. A total uncertainty of ±3% (fractional) is associated with measured short circuit currents and device efficiencies under AM1.5 illumination, as open circuit voltages are comparatively insensitive. This uncertainty is generally exceeded by device-to-device variation that is reflected in the data presented.

As in the earlier study,[8] the local EQE measurements used a focused 532 nm laser that was scanned over the device using a piezoelectric stage while the short circuit current (I_{sc}) was monitored. Laser power at the sample was maintained at (1−10) nW; total uncertainties on stated power are ±3% based on the measured change of beam intensity over the duration of the mapping experiments. The associated incident power densities are of the order 0.1 W/cm^2 based on the beam diameter of 1.5 μm, observed visually; the spatial distribution of the beam intensity was not quantified. The power density, although not the monochromatic spectral composition, is thus similar to the 0.1 W/cm^2 value of spectrally integrated AM1.5 solar insolation. Because edge diffusion effects are likely significant due to similar illumination spot size, feature dimensions, and characteristic transport lengths, the values in the EQE maps are not considered

Table 1. Performance Parameters of the Highest Efficiency Interdigitated Back Contact CdSe/CdTe Solar Cells for the Specified Width of the CdSe Contact

CdSe electrode width (μm)	V_{OC} (mV)	J_{SC} (mA/cm^2)	fill factor (FF)	efficiency, η (%)	R_{Shunt} (Ω·cm^2)	R_{Series} (Ω·cm^2)
1.0	608	15.9	52	5.00	383	12
1.5	645	15.4	55	5.47	1247	11
2.0	654	16.7	49	5.36	584	12
2.5	650	16.5	55	5.89	686	10
3.0	649	16.9	48	5.25	1247	11

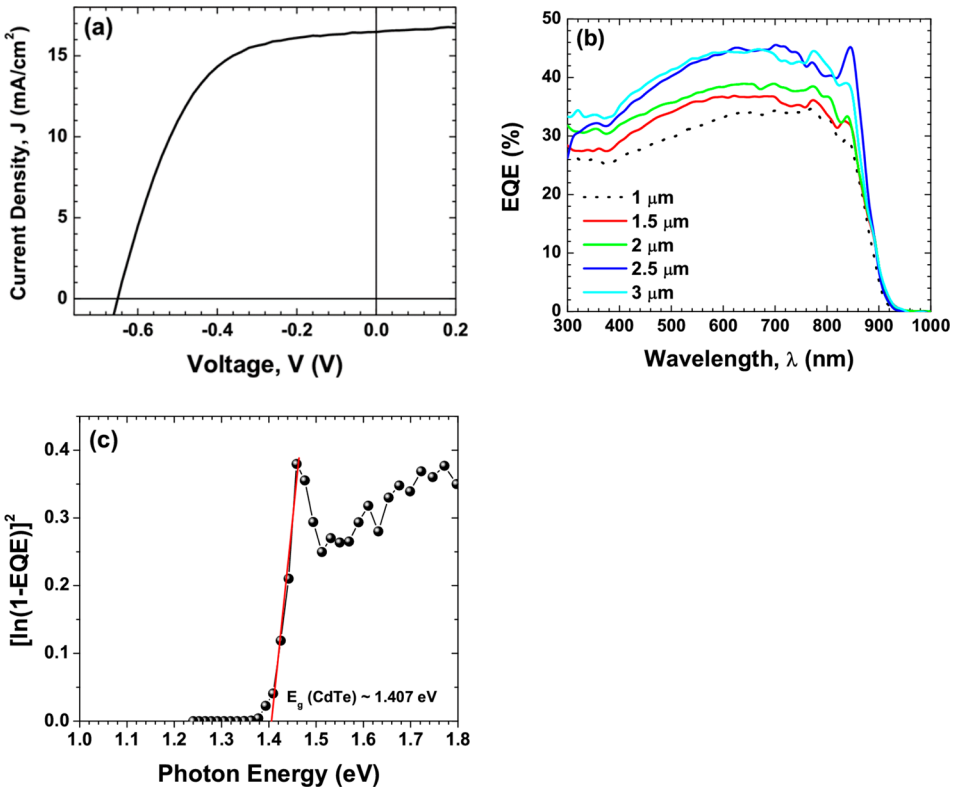

Figure 2. (a) Current density versus voltage (J–V) response of the highest efficiency CdSe/CdTe device under AM1.5 illumination. The device has 2.5 μm wide CdSe contacts. Contact lines are approximately 80 nm tall. Performance represents the highest efficiency after cumulative passivation in 40% $(NH_4)_2S$ for 30, 45, and 60 s. (b) External quantum efficiency (EQE) versus wavelength of illumination for devices with the indicated CdSe contact widths (W_{CdSe}). (c) The bandgap is indicated in a plot of $[\ln(1 - EQE)]^2$ as a function of excitation energy for the device with W_{CdSe} = 2.5 μm. All devices have 1 μm gap and 1 μm wide CdTe contacts.

directly comparable to standard external quantum efficiency measurements.

RESULTS AND DISCUSSION

Device Performance. Table 1 presents performance metrics of the highest efficiency CdSe/CdTe device for each of the CdSe electrode widths examined. The values are obtained from the J–V response under AM1.5 illumination. The scaled series resistance during operation was extracted from dV/dI, evaluated at the open circuit voltage (V_{oc}), and multiplied by the 0.16 cm^2 device area. The scaled shunt resistance was extracted from dV/dI, evaluated near zero voltage, and multiplied by the device area. The response of the device with the highest efficiency (η), a device with W_{CdSe} = 2.5 μm, is shown in Figure 2a. Figure 2b shows representative EQE response for devices with different values of W_{CdSe}. Figure 2c shows $[\ln(1 - EQE)]^2$ versus the excitation energy for the device with W_{CdSe} = 2.5 μm; the linear intercept of the absorption edges yields a bandgap of slightly over 1.4 eV (880 nm). Performance metrics are presented in Figure 3 for the four devices of each geometry exhibiting the highest efficiency.

The annealed and passivated devices exhibit no statistically significant dependence of V_{oc} on W_{CdSe} for either the best-performing devices (Table 1) or the broader set of specimens (Figure 3). The ammonium sulfide passivation[23,24] was generally responsible for 140–170 mV improvement of V_{oc}; however, only a 100–120 mV increase upon passivation was observed for some of the lower efficiency devices. Short circuit current densities range from 15.3 to 16.5 mA/cm^2 for the highest efficiency devices; all exceed published values for back contact thin film devices.[4−8] For the broad set of devices, although J_{sc} exceeds 17 mA/cm^2 for larger W_{CdSe}, the variation with W_{CdSe} is not statistically significant. The fill factor (FF) also exhibits no statistically significant variation with W_{CdSe}. Combining the three parameters, $\eta \geq 5.0\%$ is achieved by devices of each dimension, exceeding the 4.3% previously obtained with back contact thin film devices,[8] again with no statistically significant dependence on W_{CdSe}. Analysis of the data including measured CdSe and CdTe thicknesses of each

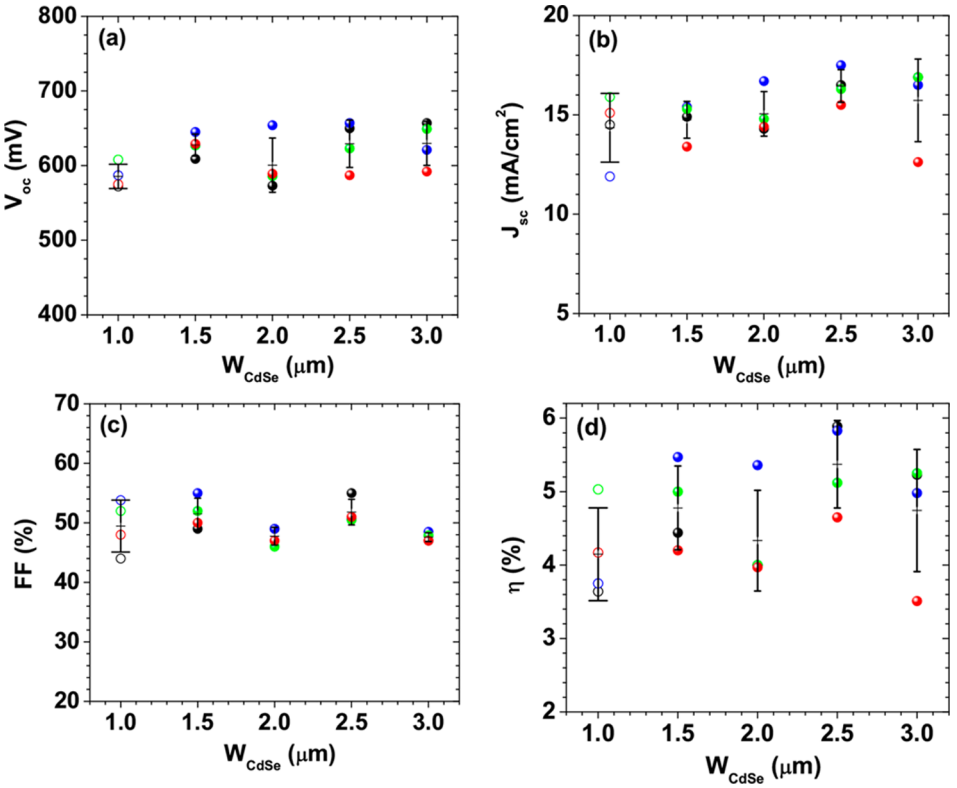

Figure 3. Plots summarizing (a) open circuit voltage, V_{oc}, (b) short circuit current density, J_{sc}, (c) fill factor, FF, and (d) device efficiency, η, under AM1.5 illumination of the back contact CdSe/CdTe devices. Results are shown for the four highest efficiency devices of each CdSe contact width W_{CdSe}. Average values with $\pm 1\sigma$ are also indicated. All devices have 1 μm wide CdTe contacts and 1 μm gap between adjacent electrodes. The asymmetric devices have ≈80 nm tall electrodes. The symmetric devices are differentiated by open symbols (○) to emphasize Ir contact thicknesses ranging from 50 to 80 nm (as well as thicker CdTe); the highest efficiency device has 70 nm thick electrodes and 0.9 μm thick CdTe. Parameters are those associated with the highest efficiency after cumulative passivation in 40% $(NH_4)_2S$ for 30, 45, and 60 s. Symbol colors are only a guide to link the properties of each device in the four plots.

device indicates no statistically significant influence on V_{oc}, J_{sc}, FF, or η for the limited thickness ranges included in the specimen set.

The EQEs of representative devices presented in Figure 2b, reaching 47%, also exceed the 39% value achieved with earlier devices. They exhibit a maximum near 650 nm that suggests absorption losses at longer wavelengths, also observed with planar "ultra thin film" devices having similar CdTe thickness,[25] as well as recombination near the surface at the shortest wavelengths. However, there is no decrease of EQE associated with the 709 nm absorption-edge of the CdSe such as is observed above the CdS absorption-edge for planar devices having a CdS window layer. As there is positive and negative variation of the stated values upon exploration of the 4 × 4 mm devices using the millimeter-size spectral light source, the values stated are those obtained at the center of each device.

Scanning Photocurrent Microscopy. Devices were characterized using the focused 532 nm laser beam in an effort to understand the charge transport and improved current density. Spatial variation of the device response is explored at the micrometer scale by mapping photocurrent response with the piezoelectric stage for laser power less than 10 nW; this maximum is estimated to yield local intensity that is four times that of spectrally integrated AM1.5 solar insolation. The maps that result, examples in Figure 4a, show that the maximum response extends from the edges of the wire contacts into the gaps between them. There is reduced response over both contacts. The device with W_{CdSe} = 2.5 μm is the same device imaged in Figure 1. Plots of the photocurrent along a line perpendicular to the contact lines (Figure 4b) reveal the nature of collection for illumination between the wire contacts and over the CdSe contact. The recombination length can be evaluated from the slope of the response moving from the junction.[26]

Performance of the nominally identical pairs of adjacent contacts in Figure 4a exhibits significant variation across the device that is especially evident with the W_{CdSe} = 1.5 μm device on the left. This reflects nonuniformity and nonconformality of the CdSe electrodeposits that are more evident on some Ir electrodes than on others (Figure 4, panels c and d, respectively).

Modeling. Quantitative modeling results can be found in the literature for 3D patterned photovoltaic geometries[14,16,27] including EQE predicted for CdTe-based devices with this back contact geometry.[4,7] The shape of the experimental EQE in Figure 2b is similar to earlier experimental results for CdSe/CdTe devices[7,8] but at higher values that are consistent with the increased J_{sc}. Compared to the earlier simulations,[4] the data suggest a corresponding increase of carrier lifetime from a low 10^{-11} s value to a value near 10^{-10} s (Figures 1 and 2 of ref 4). EQE predictions using the same materials properties[4] with bulk CdTe parameters[28] are shown for devices with W_{CdSe} = 1.0 and 3 μm in Figure 5 for a range of carrier lifetimes. Comparison of the predictions and the experimental data in Figure 2b also indicates a carrier lifetime near 10^{-10} s. The EQE is predicted to change modestly with the values of W_{CdSe} examined

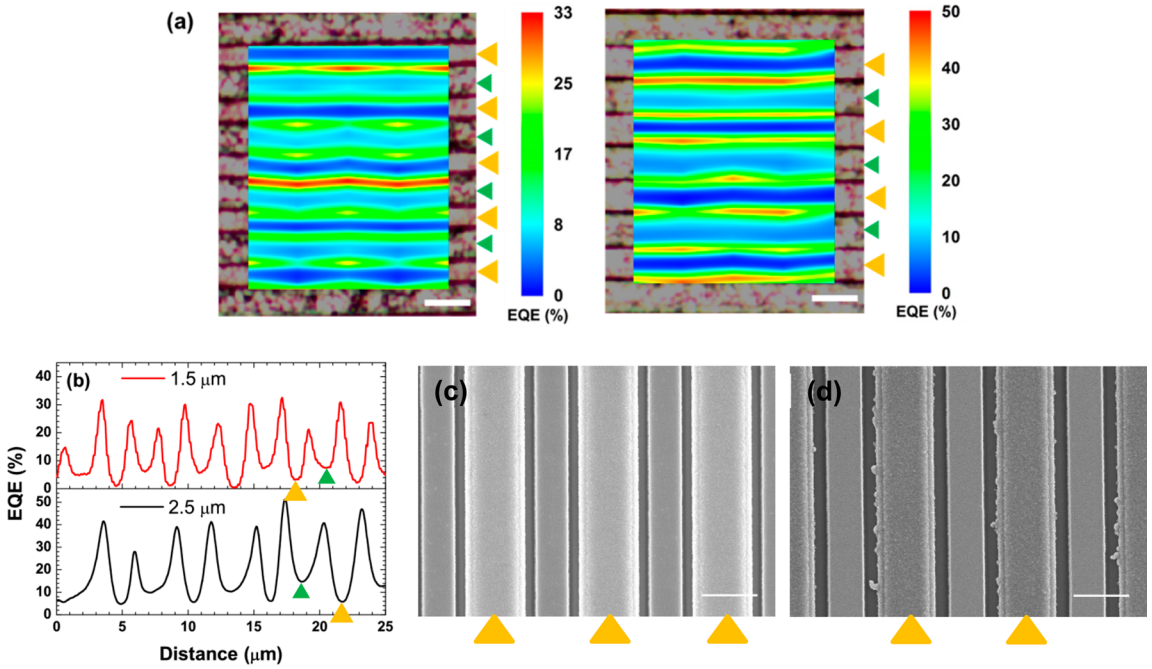

Figure 4. (a) Photocurrent maps under short circuit conditions of devices having (left) 1.5 μm and (right) 2.5 μm CdSe contact widths obtained with localized illumination at 6.7 and 7.2 nW laser power, respectively. Arrows mark the locations of the wire contacts: (large yellow ▲) CdSe contact and (small green ▲) CdTe contact. Scale bars are 4 μm. (b) Photocurrent response as nominal EQE along representative line scans perpendicular to the contact lines from the same devices, the CdSe contact widths indicated in each. Arrows (▲) mark the locations of a pair of wire contacts. Planview images of devices without overlying CdTe showing comparatively (c) conformal and (d) nonconformal growth of the CdSe electrodeposits on alternate electrodes (▲), scale bars 2 μm.

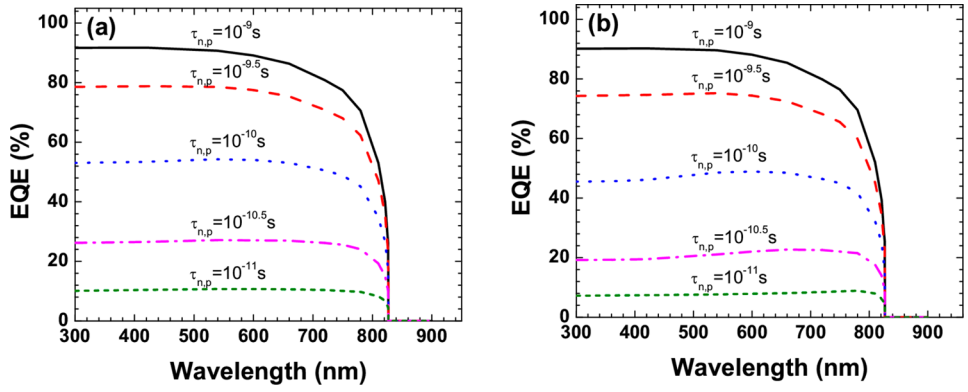

Figure 5. Model predictions of EQE under uniform illumination for different carrier lifetimes: (a) device with CdSe contact 1.0 μm wide and (b) device with CdSe contact 3.0 μm wide.

experimentally; the predicted impact of varying the contact width from 1.0 to 3.0 μm is modest compared to the impact of changing the carrier lifetime by a similar multiple.

Recombination velocity on the surface (and other interfaces) is set to zero in these simulations. Its inclusion would accentuate the decrease of EQE at the shortest wavelengths. The modest decrease predicted at these wavelengths in Figure 5 is only due to the greater travel distance to the junction for the carriers they generate near the surface.

Predicted current response, normalized by photon flux of the LBIC (i.e., local EQE), is shown as a function of probe position in Figure 6a for the device having W_{CdSe} = 1.0 μm. The predictions were generated with the 532 nm probe beam (AM1.5 power density) approximated by uniform illumination across a region 150 nm wide using the blanket EQE-obtained carrier lifetime and the bulk CdTe parameters. Figure 6b,c presents the distributions of holes and electrons contributing to the predicted photocurrent of the device for illumination at the two indicated locations in Figure 6a. The predicted response is strongly influenced by the lower value of hole mobility as compared to electron mobility in CdTe, values of 60 vs 500 $cm^2/V{\cdot}s$, respectively (confirmed by simulations using equal mobilities, not shown). Thus, illumination too far from the CdTe contact (i.e., toward the center of the CdSe contact) is predicted to yield poor current collection due to the longer distance the holes must travel; collection is predicted to improve as illumination nears the CdTe contact, so that the holes have a short travel distance and the current through the majority of the device is carried by the electrons. That said, the collection distance from the center of the CdTe contact is still quite large compared to the diffusion distance permitted by even the long electron lifetime, and the performance there is

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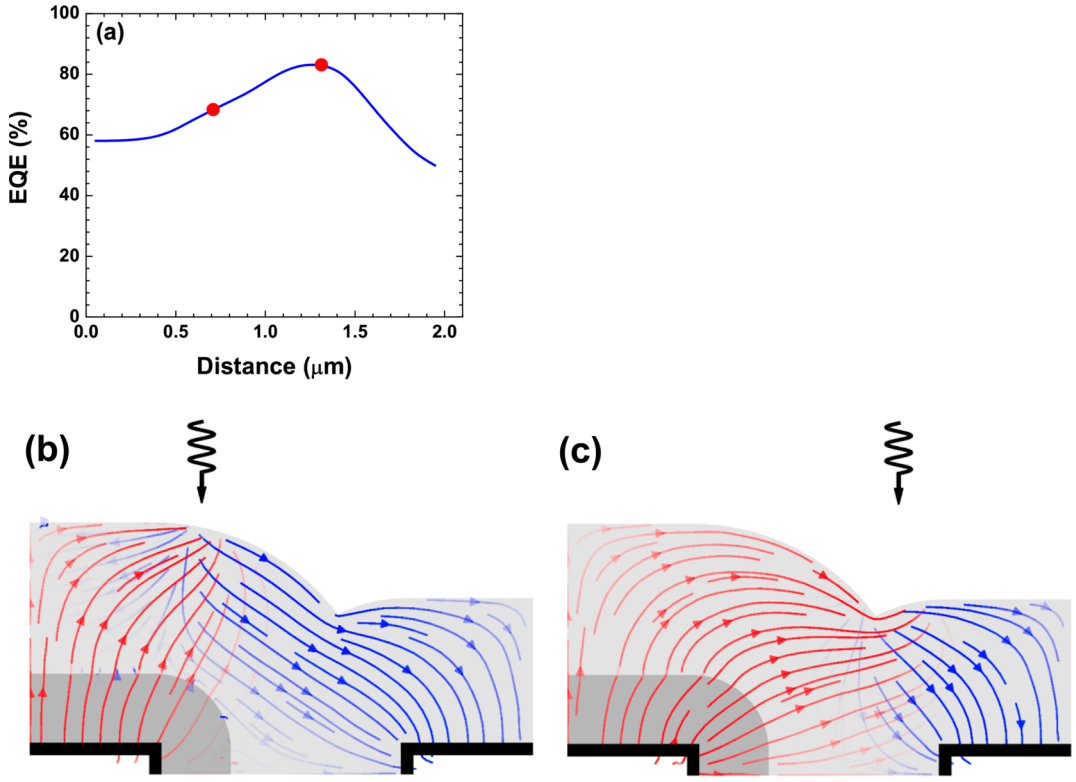

Figure 6. (a) Model predictions for the spatial variation of local EQE versus the distance of a 150 nm wide probe of 0.1 W/cm^2, 532 nm light from the middle of the CdSe electrode for a device with 1.0 μm electrodes. (b and c) Current density of electrons and holes contributing to the measured photocurrent for illumination at locations indicated by the dots in panel a: (red) electron current and (blue) hole current. The spatial range of panel a is coincident with the figures in panels b and c.

predicted to succumb to the increased recombination that comes with larger distance to the charge separation afforded by the junction.

DISCUSSION

The results of this study show improved performance of the back contact devices albeit there is no statistically significant variation of device performance with the value of W_{CdTe} in the asymmetric electrode design. As per Table 1 and Figure 3, the asymmetric geometries yield higher efficiency devices than the 5.0% value obtained with symmetrical contact lines (as well as the 4.3% value obtained previously[8]) for all values of W_{CdTe}. The highest J_{sc} value obtained exceeds 17 mA/cm^2 under AM1.5 while the highest efficiency devices exhibit values ranging from 15.3 to 16.5 mA/cm^2, approximately 53−57% of the ≈29 mA/cm^2 theoretical maximum for CdTe's ≈ 1.5 eV room temperature bandgap (and somewhat less for the apparent ≈1.4 eV bandgap). The improved performance of the best devices is associated with higher V_{oc}, J_{sc}, and FF.

The average EQE values obtained from integrating the LBIC curves in Figure 4b across the devices are only approximately 30−40% of the blanket illumination values in Figure 2b. In fact, only the maxima of the local EQE values reach the blanket illumination EQE values. As noted previously, this measurement approach is at best semiquantitative because of edge diffusion effects arising from the similar illumination spot size, recombination length and scale of the contact pattern, among other complications and approximations. For this reason, the qualitative consistency of the predictions in Figure 6a and the experimental observations in Figure 4, specifically the higher efficiency between electrodes and lower efficiency over the CdSe-coated electrode even with its p−n junction, is deemed more significant.

The simulations in Figure 6 capture the higher performance between electrodes that is observed experimentally. The 1.0 × 10^{-10} s lifetime was selected because it gives EQE ≈ 55% for blanket AM.1.5 illumination (Figure 5), which is closest to the ∼47% experimental values (Figure 2). However, it yields local response mainly ranging from 60 to 80% in the predictions for localized illumination (Figure 6a) and correspondingly higher spatial average. The nonlinear nature of recombination underlies the difference between the averages for local and blanket illumination; the larger densities of electrons and holes under uniform illumination results in a larger fraction of generated photocurrent being lost to recombination. This is of practical concern. However, understanding the spatial variation of current collection observed in the LBIC measurements of these devices, as well as the still relatively low J_{sc} observed under AM1.5 illumination, will require more detailed modeling to separate transport limitation due to recombination in the bulk of the CdTe absorber from that arising from recombination at the contacts, junction, and surface.

The decreased collection efficiency over both contacts contrasts with results previously obtained under local AM1.5-like illumination of a device with 1 μm contacts for both CdTe and CdSe, where response was indicated to be reduced most significantly over the CdTe contact.[8] This might reflect ambiguity in that interpretation (CdSe and CdTe contacts having equal electrode widths) or the substantially longer collection lengths for holes generated over the wider 1.5 and 3 μm wide CdSe contacts imaged in this study. Recombination of generated carriers is likely compounded by screening of carriers

rejected from the $p-n$ junction and CdTe contact under local illumination intensity estimated to be two to three times the AM1.5 intensity of the $J-V$ measurements. CdSe/CdTe interdiffusion, possibly manifesting in the smaller CdTe grain size over the CdSe contacts (Figure 1), might also increase local recombination rates.

The J_{sc} is reduced by the behavior over the contacts, whose combined areas is 50% of the device area for W_{CdSe} = 1 μm and 67% of the device area for W_{CdSe} = 3 μm. The efficiency of the best devices appears to improve slightly with increasing W_{CdSe}; if this is more than just statistical sampling noise, it might be associated with contact limitations. Specifically, performance limited by transport will degrade as path lengths increase with W_{CdTe}, and performance limited by recombination at interfaces will degrade as junction and contact areas increase with W_{CdTe}. In contrast, performance limited by charge transfer across contacts that are at best unoptimized (CdTe−Ir) and at worst diode-like and reverse biased (Ir−CdSe) will improve as contact area increases with W_{CdSe}.

Significantly, the areas of the highest efficiency device, W_{CdSe} = 2.5 and 1 μm wide CdTe contacts, including their sides, have just 49 and 22% of the corresponding n and p contact areas of planar devices of equal projected area. The J_{sc} of ≈17 mA/cm^2 of the best device thus corresponds to current densities greater than 65 and 35 mA/cm^2 at the CdTe and CdSe contacts, respectively. Low acceptor concentrations in the intrinsic CdTe likely impact junction and device performance at these current densities.

The asymmetric devices of this study exhibit significant improvement over the 4.3% efficiency of previously fabricated symmetric devices. However, within the uncertainty of the measurements, the highest efficiencies (5.25−5.89%, Table 1) are independent of the CdSe contact width. Instead, the higher performance is attributed to improved dimensional control provided by stepper lithography of the asymmetric devices. The tighter dimensional tolerance places a well-defined lower limit on the size of nonuniformities that impact device performance. This reduces shunting from unintended bridging or near-bridging of the CdSe electrodeposit to the CdTe contact arising from nonuniformity of the electrodeposited CdSe visible in Figure 4d. In contrast, devices fabricated using contact masks in previous studies experience additional shunting in regions with more substantial subtarget gap width between electrodes. This conclusion is supported by the lower V_{oc} and performance of symmetric devices (W_{CdSe} = 1 μm) fabricated using the contact mask in this study.

While the device efficiency remains low in comparison to values for planar thin film devices, this is a problem shared with other inorganic devices implementing advanced nanowire, nanopillar, and nanocone architectures. Compared to devices with such geometries, the 5.9% efficiency achieved here: exceeds efficiencies of devices fabricated from Si,[29] CIGS, and CdS on ZnO,[30] Cu_2ZnSnS_4 on ZnO,[31] and CdTe on ZnO;[32] matches efficiencies of devices fabricated with CdTe on CdS;[27,33] and approaches the 6.1% efficiency of CIGS on CdS[34] and 6.5% efficiency of CdTe on CdS[35] devices. While the highest efficiency is substantially exceeded by devices with elongated geometries yielding 8.2% with amorphous silicon,[36] 13.7% with Si[37] and 13.8% with InP,[38] these devices take advantage of epitaxial materials obtained by etching[39] or growth and $p-i-n$ designs that are not options for many materials and heterojunction combinations.

It is significant that the junction layer in the highest efficiency chalcogenide devices described above is CdS, as its use should permit higher V_{oc} than is possible with the CdSe used here. Also, models[4] and experiments[33] agree that features with higher aspect ratios than those of the electrodes used here (height/width < 0.1) can enhance J_{sc} and device efficiency. Past and present results thus suggest further improvement to the performance of back contact devices of the geometry examined here is possible. Approaches to be considered include

(1) taller and narrower electrode wires for larger contact and junction areas and more illumination between the contacts;
(2) scaling (with improved uniformity of electrodeposition) that enables reduced lateral dimensions (i.e., contact width, gap, and pitch);
(3) modified contact material(s), possibly including the addition of a $p+$ layer around the absorber contact;
(4) CdSe replacement by CdS or other n-type material to enable higher V_{oc}; and
(5) an absorber with improved transport properties.

CONCLUSIONS

This work demonstrates CdTe photovoltaic devices with a back contact geometry having two interdigitated comb electrodes and n-type CdSe. Device performance was improved over previously detailed performance for devices with a range of CdSe contact widths. The improvement likely arises from improved dimensional control in the lithographic patterning, which reduces localized bridging by the CdSe layer that shunts the electrodes and degrades device performance. As a result, devices achieved efficiencies under AM1.5 illumination reaching 5.9%. The best-performing devices exhibit short circuit current exceeding 17 mA/cm^2, open circuit voltage of 650 mV, or fill factor of 55% under AM1.5 illumination. External quantum efficiencies exceed 45%, with modest reduction at the longest and shortest wavelengths. Measurements, including with submicrometer resolution, suggest that variation of device performance in this study is likely dominated by variation of CdSe deposit uniformity between devices, while carrier lifetime and contact resistance limit performance.

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Notes

The authors declare no competing financial interest.

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